(12) EUROPEAN PATENT APPLICATION

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(54) **Parallel frame synchronization circuit.**

(57) A parallel frame synchronization circuit converts an incoming serial bit stream containing frame synchronization information into parallel data words on arbitrary boundaries of fixed bit length. Detectors (32, 34) forming part of the present invention determine from the parallel converted data the presence of synchronization information so as to align the incoming serial data into parallel data aligned on frame boundaries by manipulating parallel words.

The present invention is particularly suited for fabrication in complimentary metal oxide silicon (CMOS) technology and in a preferred embodiment is used to synchronize incoming data comporting to the synchronous optical network (SONET) telecommunication standard.

FIG 3
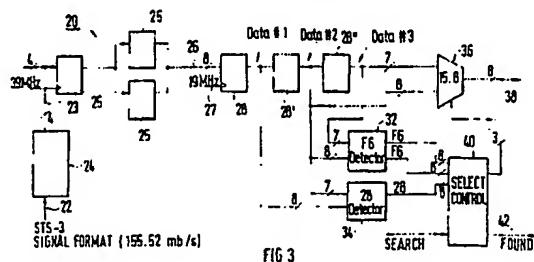
Parallel Frame Synchronization Circuit

The present invention relates to a frame synchronization method and circuit for comparing a known framing pattern to an incoming serial bit stream which contains periodic frame synchronization information so as to determine frame synchronization of the incoming data and further wherein the incoming data is first converted into parallel data of a fixed length in order to perform the frame synchronization determination with lower speed circuitry than that of the incoming serial data.

Generally frame synchronization of an incoming serial bit data stream is performed by comparing a known framing pattern to the incoming data which contains periodic frame synchronization information so as to determine the frame boundary (start of frame) based upon matching the frame synchronization information to the framing pattern.

As the speed of the data stream increases, faster logic circuitry must be used to process the incoming data. For applications in which the serial bit stream is operating at frequencies above approximately 50 megahertz, emitter coupled logic (ECL) or gallium arsenide (GaAs) fabrication technologies must be used rather than complimentary metal oxide silicon (CMOS) technology due to CMOS'S inability to operate at such speeds. ECL logic typically uses approximately ten times the power that an equivalent CMOS circuit would use which consequently requires a larger power supply and further requires additional design considerations due to the heat generated by such integrated circuit components, all resulting in a larger and more expensive circuit design than that which would otherwise be achievable using equivalent CMOS circuitry. Similarly, GaAs technology is much more difficult to fabricate than CMOS technology, resulting in much higher fabrication costs.

The present invention addresses the speed limitations of CMOS circuitry to perform frame synchronization detection of an incoming high speed bit stream which otherwise would be beyond the speed capabilities of CMOS circuitry by dividing the incoming bit stream into a plurality of parallel words, each word containing "N" bits where "N" is an integer greater than 1. Thus if N equals 4, the incoming high speed data would be divided into 4-bit parallel words with the operating frequency of such 4-bit words being exactly 1/4 the incoming data bit stream.

The circuitry contains multiple (N) frame detectors. Each detector compares the bit pattern of the incoming parallel data to a known framing pattern. Each frame detector compares the incoming parallel data from a different starting bit location so that if the incoming parallel data contains a bit pattern matching the known framing pattern, it will be detected by one of the detectors during one comparison cycle. In this manner boundary of the incoming data is determined.

This process is repeated for new incoming parallel data until the synchronization information is detected. If the detectors are comparing only a first portion of the synchronization information to a known bit pattern, then the remaining synchronization information is compared to a second known bit pattern immediately following detection of the first portion of the synchronization information.

This process can be repeated for as many units of synchronization information that are used per frame of data. Once a desired amount of synchronization information has been detected, the starting bit location within the incoming parallel data is used to identify the boundary for the incoming frame of data and all subsequent frames of data.

Once synchronization detection has occurred, the verification that synchronization information is received for subsequent frames is easily performed by the detectors observing the incoming parallel converted data at the precise time intervals when such data should be present.

It is this use of unsynchronized parallel data based upon an incoming high speed bit stream which distinguishes the present invention from other synchronization methods wherein a high speed data stream is observed without parallel conversion of the data prior to determining synchronization. The parallel word is generated without regard to frame or byte boundaries of the incoming data.

A parallel frame synchronization circuit and method according to the present invention is used to determine the location of frame synchronization information of an incoming high speed stream of data. Since such high speed data, when operating in the 50 megahertz frequency range, requires use of emitter coupled logic or gallium arsenide fabrication technologies, the present invention is able to use significantly less expensive complimentary metal oxide silicon (CMOS) circuitry by first converting the incoming high speed bit data into parallel data words which effectively reduces the operating frequency for observing the parallel data. The operating frequency reduction is proportional to the number of bits comprising each parallel data word.

For example, if the high speed bit stream is converted into parallel words where each word comprises 4 bits, then the frequency of this 4-bit data is 1/4 that of the high speed serial data. Due to this lower operating frequency of the parallel

data, it is feasible to use CMOS circuitry in situations where the high speed data is operating at the 100 megahertz or higher frequency range. The present invention is applicable with any size parallel data, although the preferred embodiment of the invention as set forth herein, divides the incoming data into 8 bit words.

In order to perform synchronization information detection, it is necessary that the known bit pattern be compared against the parallel data for every possible starting location of the parallel data.

For example, if the incoming serial bit stream is divided into arbitrary 4-bit parallel words and if the synchronization information is 4 bits in length, then in order to insure detection of the 4-bit synchronization information regardless of where within any given 4-bit parallel word the 4-bit synchronization word may begin, then four 4-bit pattern detectors would be necessary to simultaneously compare the first seven bits of two time-adjacent parallel data words. This comparison process would then be repeated for each subsequent 4-bit parallel word received.

If the synchronization information has a bit length greater than the parallel data words used by the frame synchronization detection circuitry and if a plurality of data latches are not used to allow simultaneous comparison of the entire known bit pattern to the incoming parallel data, then the subsequent portion or portions of the synchronization information can be compared to the corresponding portion or portions of a known bit pattern once the first portion of the synchronization information is detected. This subsequent synchronization information detection uses the same type of parallel bit pattern detectors as used to detect the first portion of the synchronization information . These detectors typically are additional detectors although the same detectors which detected the first portion of the synchronization information could be used if the comparison bit pattern is alterable by these detectors. In the preferred embodiment of the present invention, separate detectors are used to determine the presence of a second portion of the synchronization information.

Once all the synchronization information has been detected, then the specific starting bit location of the frame synchronization information is known via the address of the detector which found the matching synchronization information. Consequently the starting location of the frame of data is determined.

This correct data alignment is achievable through use of a data selector which uses the address of the detector which found the matching frame synchronization information so as to adjust transfer of all subsequent incoming data forming part of the frame (or subsequent frames) to be in

correct word alignment. Typically such word alignment is on an eight bit byte boundary.

From the foregoing description, it is apparent that the parallel frame synchronization circuit and method is applicable for use with any type of continuous or packet-type communication link where a known framing pattern is used at the beginning of each frame to define the location of that frame in a serial data stream.

It is therefore a principle object of the present invention to provide a parallel frame synchronization circuit which converts a high-speed serial bit stream into a lower speed parallel stream of multi-bit words, with use of a plurality of pattern detectors for comparing the multi-bit words to a known frame synchronization pattern so as to determine the location within the bit stream of the frame synchronization information regardless of the location where the incoming serial bit stream is converted into multi-bit parallel words.

For a fuller understanding in the nature and object of the present invention, reference should be made for the following detailed description taken in connection with the accompanying drawings, in which:

Figure 1 is a diagram showing the 125 microsecond frame pattern of one channel of a particular telecommunication standard known as SONET;

Figure 2 is a diagram of the SONET standard wherein information of three channels is transmitted during a 125 microsecond time period;

Figure 3 is a block diagram of the parallel frame synchronization circuit according to the invention;

Figure 4 is a detailed block diagram corresponding to Figure 3;

Figure 5 is a timing diagram corresponding to the operation of the block diagram shown in Figures 3 and 4; and

Figure 6 is a diagram that illustrates frame information detection for an F6 framing information pattern.

As seen in Figures 3 - 4, the present invention is a parallel frame synchronization circuit 20 for finding frame synchronization information embedded within an incoming serial bit stream 22.

In one application of the present invention, the parallel frame synchronization circuit is used to find framing information associated with a frame of data as illustrated in Figure 1. This type of frame comports to what is known as the Synchronous Optical NETwork (SONET) standard (American National Standards Institute, Inc. standard TI.105-1988). As seen in Figure 1, this standard comprises a standard frame format. For one channel this format is 810 bytes, wherein the bytes can be visualized as residing in nine rows, each row comprising ninety

bytes. The first three columns of each row represents what are considered overhead bytes, with the first two bytes of the first row generally designated by the names A1 and A2. Under the SONET standard, the A1 and A2 bytes of the first row contain a defined framing pattern.

The value of A1 is the eight bit pattern of 1111 0110 binary, or F6 hexidecimal. The A2 bit pattern is 0010 1000 binary, or 28 hexidecimal.

The third byte of the first row is designated by the name C1 and contains a channel identification number for the incoming data. For the SONET standard shown in Figure 1, which comprises only one channel, the value of C1 would always be 01 for each frame. Specifically, the value of C1 ranges from 1 to Z for a Z channel system.

As also seen in Figure 1, the 810 bytes of data comprising one frame of a single channel SONET standard is transmitted during a 125 microsecond time period which therefore equates to a bit transmission rate of 51.84 megabits per second [(810 x 8)/(125 x 10 $^{-6}$)].

As seen in Figure 2 for a multi-channel SONET standard, each additional channel has its 810 bytes transmitted along with the other channels, one byte at a time. Thus, the A1 byte is first transmitted for channel 1, then for channel 2, etc.. Then the A2 byte is transmitted for channel 1, then for channel 2, etc., through all 810 bytes comprising a frame for each channel. The 125 microsecond time period for transmitting all 810 bytes of all channels is maintained and consequently, the serial bit stream increases by a multiple equal to the number of channels. For the SONET STS-3 standard where three channels are used (Z = 3, see Figure 2), the bit stream rate is three times the STS-1 (Figure 1) standard and thus, is 155.52 megabits per second.

The present invention is directed to identifying the presence of framing information, which for the SONET standard is directed to finding the A1 and A2 bytes of the 810 byte frame.

For the STS-1 standard comprising one channel of information, the preferred embodiment of the present invention locates the occurrence of the A1 and A2 framing bytes (framing information). This framing information has a length P, where P is an integer equal to the total number of bits of framing information used to detect frame synchronization. For the STS-1 frame standard, P is equal to 16 (two 8-bit bytes).

For a multi-channel SONET standard, the present invention can look for a plurality of A1 or A2 bytes for one or more channels. In a preferred embodiment of the invention, two A1 bytes followed by an A2 byte are searched for the STS-3 SONET standard.

Regardless of the particular framing bytes which are examined for purposes of determining the start of frame, the present invention uses the same technique for converting the serial data into lower speed parallel data; namely, converting the incoming serial bit stream into parallel data words, each comprising N bits, where N is an integer greater than one and typically is an integer equal to a power of two.

Figures 3 and 4 show an implementation of the parallel synchronization circuit designed to find the adjacent framing bytes A1-2, A1-3 and A2-1 of a three channel SONET standard (STS-3 configuration). In this implementation the incoming serial bit stream 22 is converted to a multi-bit parallel data word 23 by means of a serial to parallel converter 24 which must operate at the bit stream rate of the incoming data. This parallel data is first four bits in length. This four bit data is then converted into 8 bit parallel data 26 by means of latches 25 so that the clock frequency is further reduced from 38.88 MHZ to 19.44 MHZ. Since the incoming data for the STS-3 standard is arriving at 155.52 megabits per second, such conversion circuitry cannot easily be fabricated using complimentary oxide silicon (CMOS) technology which generally cannot operate reliably beyond 40 to 60 megahertz. Good design practice dictates that this converter be implemented in emitter-coupled logic (ECL) technology for an STS-Z implementation where Z is greater than 1 and equal to or less than 12, and in GaAs technology, where Z is greater than 12.

As shown in Figures 3 and 4, the serial to parallel convertor 24 generates a parallel data word output 26 comprising 8 bits of parallel data per word and thus has a transmission frequency equal to 1.8 that of the incoming serial bit stream. The parallel data words are sequentially transferred to an 8-bit latch 28 under control of clock signals on input 27. Each subsequent data word causes the previous data words to be shifted to the next latch; that is, from latch #1 (28), to latch #2 (28'), to latch #3 (28″) (see Figure 6). The latches therefore act like parallel data shift registers with each latch having eight output lines 30 (only seven of these lines are necessary for latch 28″), with each output line representing the state of one of the bits in the 8-bit data word contained within the particular latch.

As also seen in Figure 3, eight first framing byte pattern detectors 32 (A1 detectors) are each connected to eight of the output lines 30 of latches 28′ and/or 28″. The first detector (detector #1) is connected to the output lines of latch #2 (28′) (output lines 0 - 7), while detector #2 is connected to output lines 1 through 7 of latch #2 and line 0 of latch #3 (line 0 of latch 3 corresponds to line 8 shown in Figure 4 connected to A1 detector #2), with this pattern sequentially increasing so that detector #8 is connected to output line 7 of latch 2 and output lines 0 - 6 of latch #3 (i.e. lines 7 -14).

The eight output lines connected to each detector are presented to each detector in parallel.

In this manner, each detector is able to simultaneously observe a unique bit pattern of eight sequential output lines of the latches. As noted above for the SONET standard, the first framing byte has the bit pattern 1111 0110 (F6 hexadecimal) and it is this bit pattern that each detector compares to the bit pattern for the output lines to which it is connected.

It is empirically observed that with eight 8-bit detectors configured as shown in Figure 3, then an 8-bit framing byte must be detected, if present, regardless of the starting bit location of the framing byte, by examining the state of the lines 0 - 14 at least once after each 8-bit data word is sequentially transferred to the latches.

Figure 6 shows an example where the data within latches 3 and 2 is as follows:
don't care data for lines 14 - 10 of bus 55 (latch #3, bits 6 - 2; note that
the letter "X" denotes any data; i.e. a 1 or a 0), the value 1 for lines 9 and 8 (latch #3, bits 2, 1), the values 1 1 0 1 1 0 for lines 7 - 2 (latch #2, bits 7 - 2), and the values 1 1 for lines 1 and 0 (latch #2, bits 1,0).

Bits 7 - 0 of latch #1 have the values 1 1 0 1 1 0 1 1. It is seen in Figures 4 - 6 that the fifteen lines of bus 53 span latch #2, bits 6 - 0 and latch #1, bits 7 - 0, while bus 55 spans latch #3, bits 6 - 0 and latch #2 bits 7 - 0. It is also seen that for the example shown in Figure 6, the A1-1 F6 framing byte (1 1 1 1 0 1 1 0 binary) span latch #3, bits 1, 0 and latch #2, bits 7 - 2 (lines 9 - 2 of bus 55) while the A1-2 F6 framing byte spans latch #2, bits 1, 0 and latch #1, bits 7 - 2 (lines 9 - 2 of bus 53).

Again referring to Figure 6, it is observed that one byte time (clock cycle) later, the A1-1 framing byte is partially beyond latch #3 and the A1-2 framing byte (see Figure 2) is present on detector #3. A second byte time later than A1-3 framing byte is present on detector #3 followed by the A2-1 framing byte (28 hexadecimal).

One byte time before the A1-1 framing byte was detected by A1 detector #3, the A1-1 framing byte would only be partially located in latch #2 (namely, the most significant 2 bits of the bit pattern 1111 0110). It is also observed that regardless of the position of the framing byte within the 8-bit parallel words, that its detection will be assured provided that detectors 32 perform a detection operation at least once per every data word transfer.

It is therefore seen that bit 7 of latch #3 is not required since if the framing byte was on an 8-bit data word boundary, and thus residing from bits 7 to 0 of latch #3, then one byte time earlier, that same framing byte would reside at bits 7 - 0 of latch #2 and thus would be detected at that time by A1 detector #1.

It is also observed that if the detection process is performed after each 8-bit data word transfer, only two 8-bit latches need be used with eight 8-bit detectors for each framing byte to be detected.

Each detector 32 has a one bit output 37 which is activated when a detection is made. Thus if detector #3 found the A1 framing byte, its output line would be active.

Each A1 detector output line is connected to a corresponding one of eight one-byte delay flip-flop 35 and to a corresponding one of eight AND gate 39. Thus the A1 detector #1 output line is connected to an input of the #1 flip-flop and to an input of the #1 AND gate 39. Each flip-flop has an output 41 which is active if the flip-flop input was active (true) one parallel clock pulse earlier. In this manner, the A1 detectors and the flip-flops can monitor two time adjacent clock cycles. The output lines 37 and 41 of a corresponding A1 detector, flip-flop pair are both active when the first and second A1 framing bytes are detected and when the second and third A1 framing bytes are detected. Figure 5 shows this occurrence.

In the preferred embodiment of the invention, two adjacent A1 framing bytes followed by an adjacent A2 framing byte are required to determine proper synchronization of the STS-3 SONET frame. Thus after two adjacent A1 framing bytes have been detected (i.e. the A1-2 and the A1-3 bytes), an A2 framing byte (the A2-1 framing byte) must be detected. This is performed by eight A2 detectors 34 whose operations are similar to those of the A1 detectors 32 except that they monitor the outputs of latches 28 and 28' (latch #1 and #2). Each A2 detector has a one bit output 43 which is connected to one input of the corresponding AND gate 39. Thus only one of the eight AND gates 39 has its output 45 enabled when the A1-2, A1-3, A2-1 framing byte sequence is detected (see Figure 5). This particular AND gate output instructs encoder 46 to generate a three bit output signal on lines 47 which identify the AND gate number and thus the framing byte boundary.

This signal is presented to a latch 48 which in turn presents the identifying information on its three line output 49 to data selector 36. Data selector 36 then selects the corresponding eight lines from latches 28' and 28" which correspond to the AND gate number. For example, if AND gate #3 has an enabled output, this represents A1 and A2 detection by corresponding detectors #3 which span lines 9 - 2. These lines are then selected by data selector 36 and presented an output 38.

The AND gates 39 in combination with encoder 46, latch 48 and logic gates 50 and 51 comprise a comparator circuit 40. Output line 42 is enabled

when framing synchronization has been detected.

Based upon the previous example, it is seen that the mathematical expression defining the number of detectors (R) necessary to detect a unit of framing information is equal to the size of the incoming parallel data word times the sum of the truncated integer value of the quotient of the frequency of such parallel data words (f_{pdw}) divided by the frequency at which detector comparisons (f_{dc}) are made plus one (plus one if f_{pdw}/f_{dc} has a remainder). That is:

R = No. of detectors = N x [truncated value of (-(frequency of incoming parallel data words)-/(frequency of detector comparisons)) + 1 if f_{pdw}/f_{dc} has a remainder]; or

R = No. of detectors = N x {trunc[f_{pdw}/f_{dc}] + 1 (+ 1 if f_{pdw}/f_{dc} has a remainder)}.

For example, if N equals 4 and if the frequency of detector comparisons is equal to 1·2 the frequency of the incoming parallel data words, then the minimum number of detectors necessary is

R = No. of detectors = 4 x [truncated value of (1/0.5) + 1 if a remainder is present] = 4 x (2) (no remainder) = 8 detectors.

Since the frequency of detector comparisons (f_{dc}) of the data within the latches is not meaningful if performed at a frequency greater than that of the incoming parallel data words (since in such a case the parallel data words would not change between consecutive comparisons until such time as the parallel data word in fact changes), then the minimum number of detectors necessary when the frequency of detector comparisons is at least equal to the incoming parallel data frequency is just equal to the value of N; that is, the width of the incoming parallel data words.

From the foregoing, it is also apparent that the number of bits (Q, where Q is an integer) that each detector must observe is equal to the size of the unit of framing information desired to be detected per comparison, and as a maximum, is not larger than the total size of the framing information. The minimum size of the number of bits that each detector must observe is at least the size of the framing information (P) if the size of the framing information is equal to or less than the size of the parallel data words (N). Furthermore, if the size of the framing information is greater than the size of the parallel data words (P > N), then the minimum number of bits that each detector must observe is equal to the number of bits in the parallel data word times the sum of the truncated integer value of the quotient of f_{pdw} divided by f_{dc} plus one (plus one if the quotient has remainder), or

Q_{min} = R x {trunc[f_{pdw}/f_{dc}] + 1 (+ 1 if f_{pdw}/f_{dc} has a remainder)}.

For example, for the STS-1 SONET standard where the A1 and A2 bytes comprise the framing

information and wherein these two bytes constantly equal sixteen bits of framing information (P = 16), then the detectors as a maximum value need not observe more than sixteen bits each per detection comparison, but may detect as few as 8 bits where the incoming data is placed into 8-bit data words (N = 8) by the serial to parallel convertor 24. The minimum frequency per comparison for these two extremes is once per two 8-bit parallel word transfers and once per one 8-bit parallel word transfer respectively. In the example shown in Figure 3, each detector compares eight bits of output data which is therefore within the permissible range of between eight and sixteen bits of data.

As seen in Figure 4, the minimum number of outputs 30 (S, where S is an integer) necessary for framing information detection is equal to the number of bits (Q) associated with each detector 32 plus the number of detectors (R) necessary for framing information detection, minus one. That is,

S = minimum number of output lines = Q + R - 1.

From the foregoing, it is also apparent that the frequency of detector comparisons must at least be equal to the frequency of the incoming parallel data divided by the truncated integer value of the quotient of the number of bits compared by each detector divided by the number of bits of the incoming data words plus one if the quotient has a remainder. That is,

minimum f_{dc} = f_{pdw}/{trunc(Q/N) + 1 (+ 1 if Q/N has a remainder)}.

In other words, if the incoming data words have a size of 4 bits and if each detector is comparing a known bit pattern to 4 incoming bits of data from output lines 30, then the minimum frequency of detection must be equal that of the incoming parallel data words, for otherwise it would be possible for an incoming data word not to be observed by any detector, assuming that the minimum number of detectors is as defined above. Similarly if each detector is comparing a known bit pattern of 5 bits, then

$f_{dc(min)}$ = f_{pdw}/{trunc(5/4) + 1 if remainder is present}

f_{dc}(min) = f_{pdw}/{1 + 1}, remainder of 0.25 present

f_{dc}(min) = f_{pdw}/2, or once every two parallel data word transfers.

It is also seen from the foregoing analysis that in the unlikely event that the framing information has a bit length (P) less than that of the parallel output data (N), then the minimum number of bits (Q) associated with each detector must equal that of the framing information (P) rather than the number of bits in the parallel data words.

For example, if the framing information only comprises 3 bits (a very unlikely amount) then each detector must observe 3 bits output lines 30.

In such a situation, the minimum number of detectors must still at least equal the value of N.

Once framing determination has been made, the circuitry no longer remains in the search mode; that is, it no longer looks at every unit of incoming parallel data. Rather, the circuit determines when the next framing byte should appear. For a single channel SONET standard this reoccurrence is 810 bytes after the A1 framing byte has been detected. The frame synchronization circuit can therefore look for the A1 and A2 framing bytes at their proper time sequence and if found, can continue this process until the proper framing information is not found and if so, reenter the search mode if the proper framing information is not found for one or more sequential frames.

Although the implementations shown are directed to telecommunication implementations embodying the SONET data communication framing standard, it is apparent that the circuitry and method for parallel frame synchronization detection can be used with any continuous or packet type communication link where a known unit of framing information is used at the beginning of each frame to define the beginning of said frame.

It will therefore be seen that the objects set forth above, and those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in carrying out the above construction or method without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

Claims

1. Parallel frame synchronization circuit for detecting known frames synchronization information having a length of P bits, where P is an integer greater than 1, the frame synchronization information forming part of a serial bit stream of data having a frequency f_{in}, comprising
a serial to parallel converter (24, 25) for converting the incoming serial bit stream (22) into parallel data words (26), each word comprising N bits, where N is an integer greater than 1;
means (28, 28', 28") for receiving the parallel data words (26) from the serial to parallel converter (24, 25) so as to present their output values on a first plurality of parallel output lines (55);
a first group of detectors (32) consisting of a second plurality of detectors, each detector having a third plurality of inputs so that the plurality of detector inputs span the parallel output lines of the receiving means, wherein each detector comprises means for determining if the data presented at its

third plurality of inputs corresponds to at least a portion of the frame synchronization information so as to generate an output if a comparison is made; and
means (36) interconnected to each detector and to the parallel output lines (55) of the receiving means for generating parallel output data (38) aligned with the detection location of the frame synchronization information.

2. A parallel frame synchronization circuit as claimed in claim 1, further comprising a second group of detectors (31) consisting of the second plurality of detectors and serving to detect a second portion (A2) of the frame synchronization information after detection of a first portion (A1) of the frame synchronization information by the first group of detectors (32) the second group of detectors (31) connected to the parallel output lines of the receiving means in the same manner as the first detectors (32), and wherein the means (36) for generating a parallel output of data does not generate such an output of data until both the first and second portions of the frame synchronization information are detected.

3. A parallel frame synchronization circuit as claimed in claim 1, wherein the frame synchronization information comprises at least first and second time adjacent portions having the same information (A1, A1) and wherein the parallel frame synchronization further comprises a fourth plurality of flip-flops (35), each having an input connected to an output of one of the second group of detectors (31) and each having an output which reflects the state of its input one clock cycle earlier, and further logic means (39) for receipt of the output of each flip-flop and each output of each detector (31, 32) and the means for generating the parallel output of data aligned with the boundary of the units of data so that frame synchronization is determined when the adjacent portions of the frame synchronization information are detected by the detector and flip-flop consecutively.

4. A parallel frame synchronization circuit as claimed in any one of the claims 1 to 3,
wherein the first plurality of parallel output lines is at least Q + R-1, where Q is the third plurality of inputs of each detector with values as set forth hereinafter, and R is the second plurality of detectors with a minimum value as set forth hereinafter,
said receiving means receiving at least the truncated integer values of [(2Q/N) + 1 (+1 if (2Q/N) has a remainder)] sequential parallel data words;
wherein R is an integer at least equal to N times the sum of the truncated integer value of the quotient of the frequency of the parallel data words (f_{pdw}) divided by the frequency at which detector comparisons are made (f_{dc}), plus one (plus one if f_{pdw}/f_{dc} has a remainder), that is,

R = N x [truncated [f_{pdw},f_{dc}] + 1 (+ 1 if f_{pdw}/f_{dc} has a remainder)],

and wherein Q is equal to at least R but not greater than P if P is > N, the Q inputs of each detector connected to Q parallel output lines of the receiving means so that for each detector i, where i is an integer from 2 to Q, Q-1 inputs are connected to the same parallel output lines as detector i-1, so that the Q detectors span the 2Q-1 parallel output lines of the receiving means.

5. A frame synchronization circuit as claimed in claim 4, wherein the value of N equals 8 and Q = 8 and f_{dc} = 1/2 f_{pdw}.

6. A parallel synchronization circuit as claimed in claim 4, wherein P may have a value less than N and if P is less than N, then the number of inputs Q associated with each detector is P.

7. A frame synchronization circuit as claimed in claim 4, wherein each detector means for periodically determining if the incoming data bits correspond to at least a portion of the known synchronization information, operates at a frequency at least equal to the incoming frequency of the parallel data words divided by the sum of the truncated value of Q/N + 1, (+ 1 if Q/N has a remainder).

STS – 1
SIGNAL FORMAT
51.84 mb/s

A1, A2 framing bytes =   F6 28 (HEX)

FIG. 1

ZX 90 Bytes

9 Bytes

A1-1 A1-2 A1-3 A2-1 A2-2 A2-3 C1-1 C1-2 C1-3

ZX 87 Bytes

9 ROWS

OVERHEAD
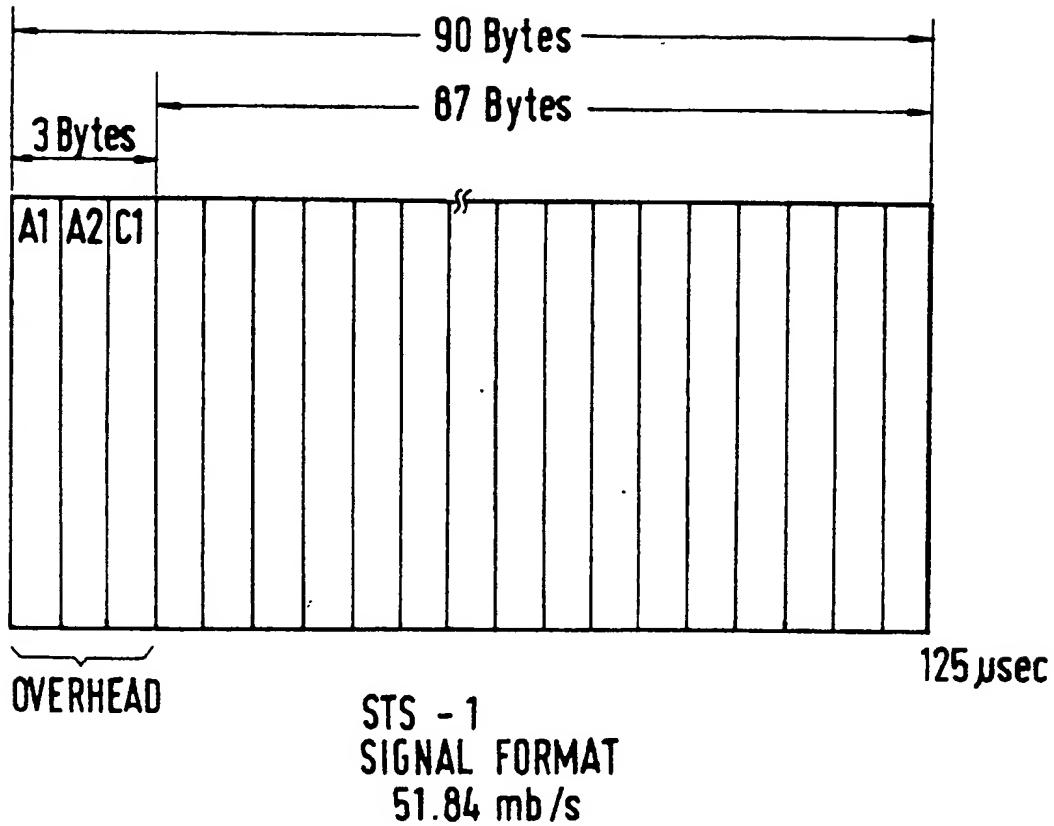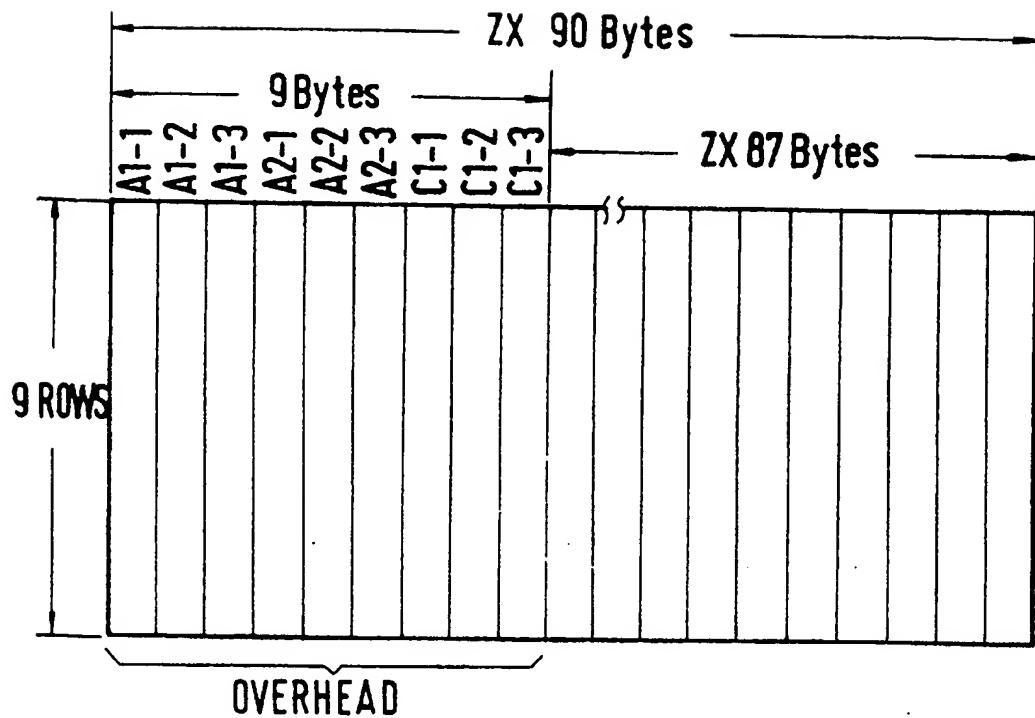
STS-3
SIGNAL FORMAT
155.52 mb/s

3 A1 bytes each = F6 (HEX)
3 A2 bytes each = 28 (HEX)

FIG. 2
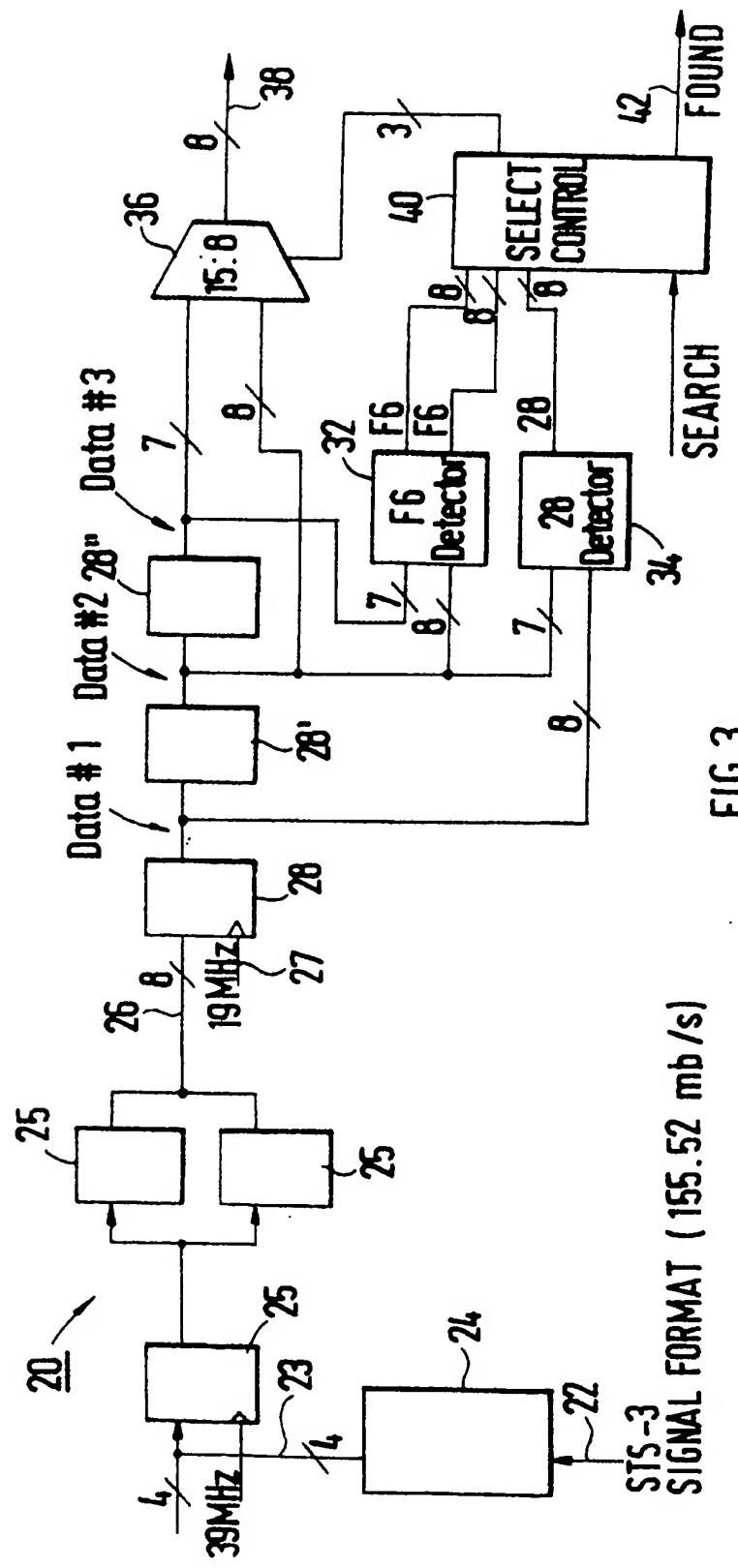
FIG.3
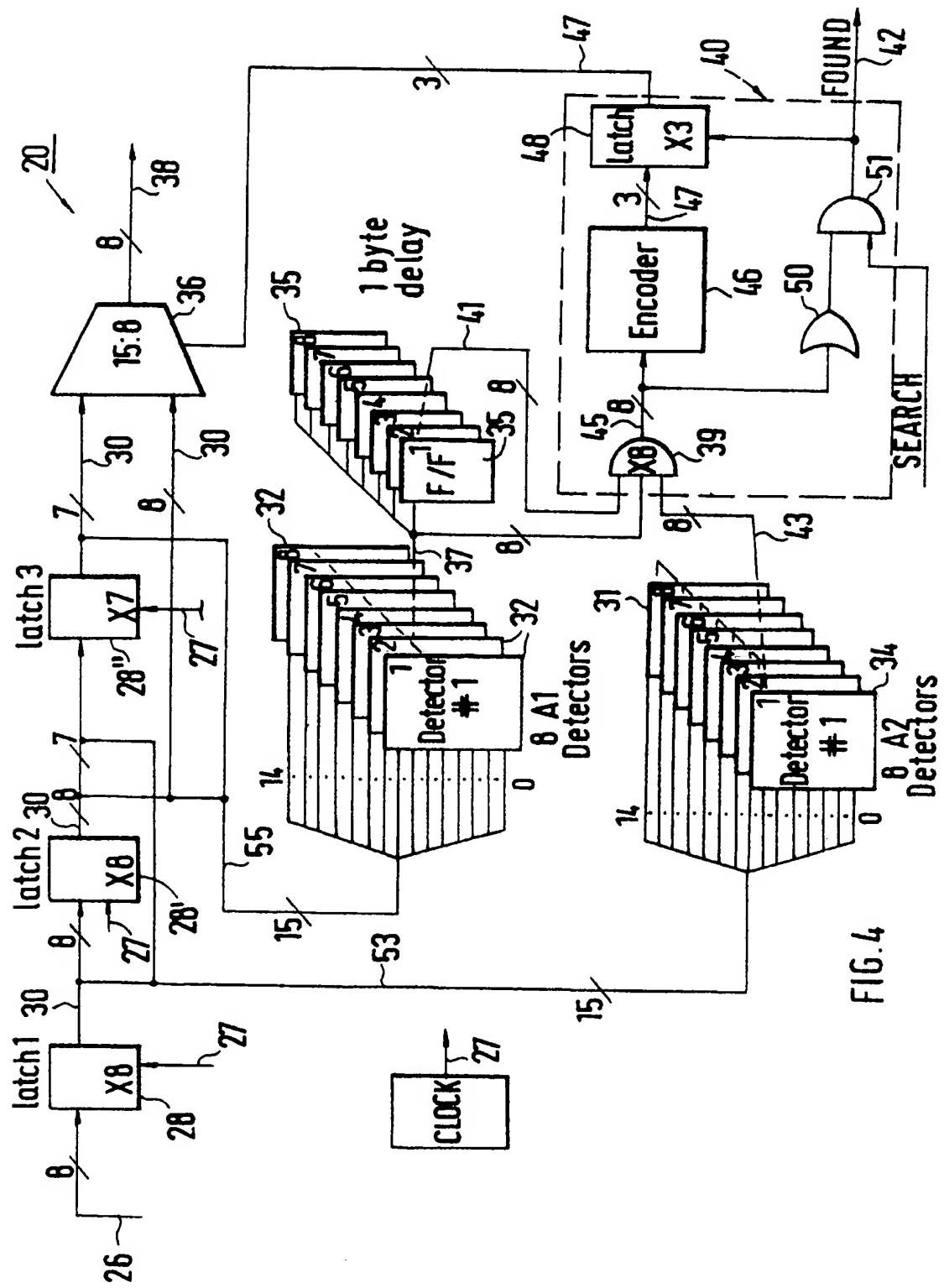
FIG.4
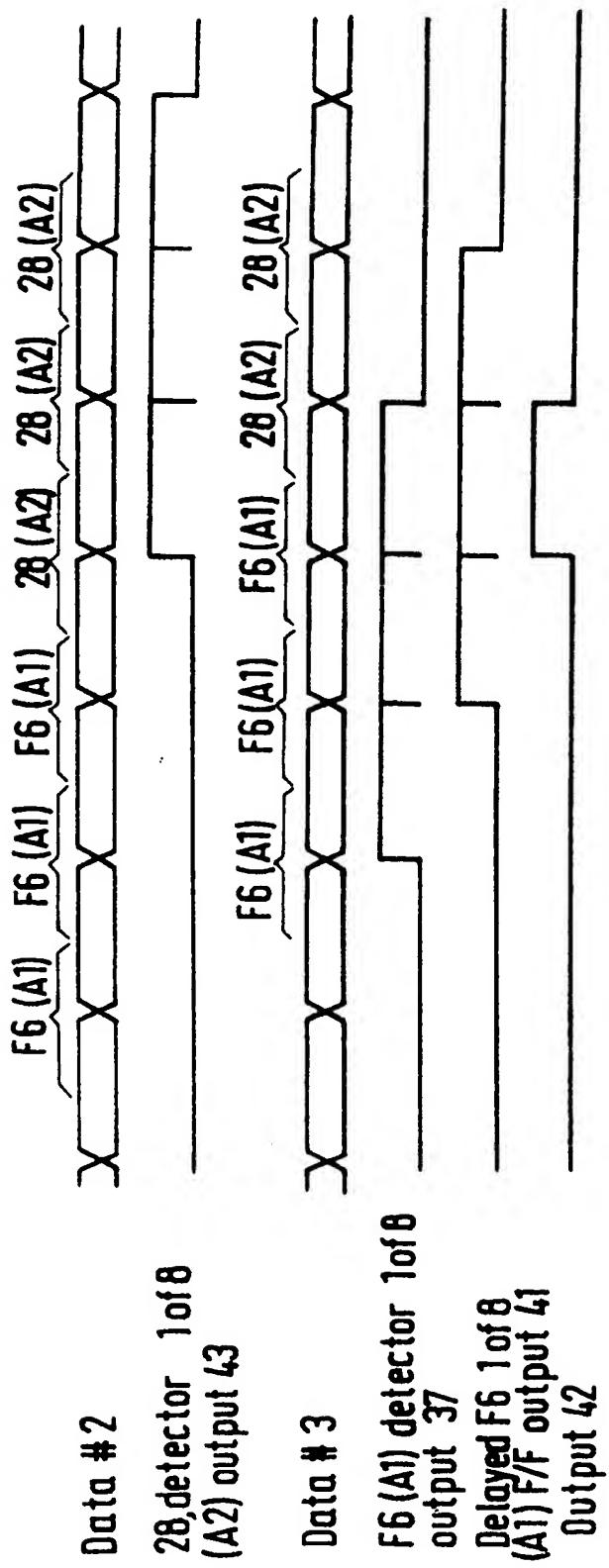
FIG.5
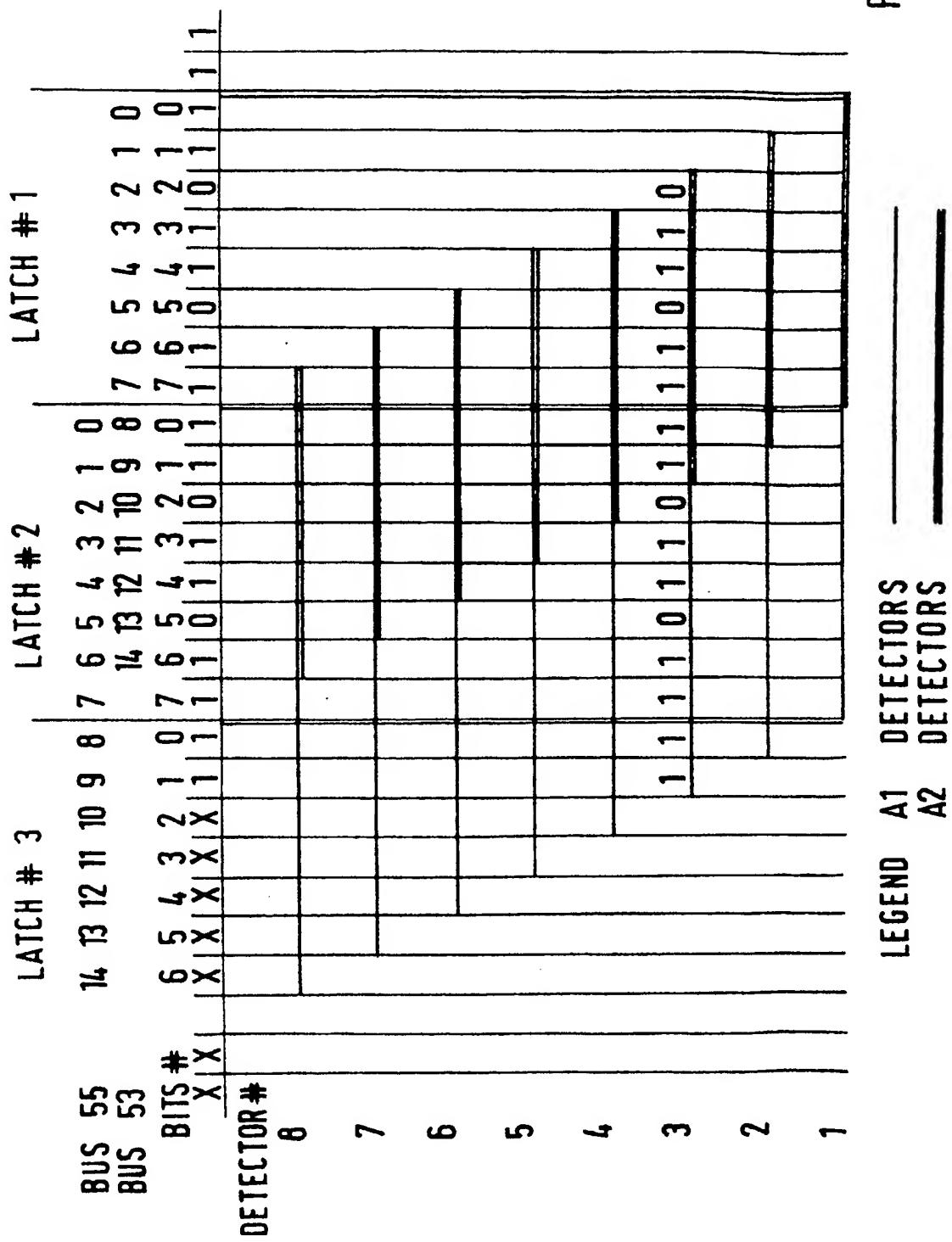
LATCH # 3   LATCH # 2   LATCH # 1

BUS 55   BITS #
BUS 53

DETECTOR #
8
7
6
5
4
3
2
1

FIG.6

LEGEND   A1   DETECTORS
         A2   DETECTORS

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	FR-A-2 538 647 (BILLY ET HENRY) * Whole document *	1	H 04 J 3/06 H 03 M 9/00
Y		2-7	

Y	EP-A-0 249 935 (FUJITSU LTD) * Whole document *	2-7	

A	EP-A-0 311 251 (WESTINGHOUSE ELECTRIC CORP.)		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 J
H 03 K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16-08-1990	SEGAERT P.A.O.M.P.